AMENDMENTS TO THE SPECIFICATION

Please replace paragraph **[0060]** with the following amended paragraph:

[0060] Tables [[5]] 4 and 5 are examples of the lookup table 52. Table 4 shows values that the lookup table 52 may substitute for modulated data values of a modulated data band, wherein the values may be derived by way of converting the source data into the 7-bit data in lookup Table 3, selecting a minimum value in a specific modulated data band that satisfies Formula (3), and selecting a maximum value in a specific modulated data that satisfies Formula (5). Specifically, the source data of Table 3 may be converted into 7-bit data. Accordingly, among the modulated data satisfying Formulas (3) and (5), *i.e.* , four modulated data adjacent to their top/bottom/left/right, the modulated data corresponding to an undershoot may be substituted for the remaining three modulated data. When the source data are modulated to a value a little lower than the optimal modulated data pre-set upon the high-speed driving, there is almost no effect on a subjective picture quality perceived by an observer, but if the source data is modulated to a value higher than the optimal modulated data, there is a sudden change in the brightness of a picture perceived by an observer. Accordingly, as the number of bits of the source data decreases, the appropriate value for the undershoot in specific modulated data may be substituted for the modulated data while maintaining a high-speed driving effect, thereby reducing the number of the modulated data to one fourth thereof. Table 5 shows a re-configured lookup table of FIG 3 by way of taking one out of [[tow]] two identical adjacent source data from Table 4.

Please replace paragraph **[0063]** with the following amended paragraph:

[0063] If the value of the 8-bit source data is an odd number in the step S1, each of the first and second converters 59A and 59B may subtract '1' from the odd data to turn the odd data into an even data (steps S2 and S3). Subsequently, in step S4, each of the first and second converters 59A and 59B may divide the converted 8-bit even data by '2' and may convert the divided data into the 7-bit data, then may supply the converted 7-bit data (in step S5) to the lookup table 52.

Please replace paragraph **[0065]** with the following amended paragraph:

[0065] FIG 8 is a block diagram representing an exemplary apparatus for driving a liquid crystal display according to a second embodiment of the present invention. Referring to FIG 8, the apparatus for driving the liquid crystal display may include a liquid crystal display panel 57 having data lines 55 and gate lines 56 crossing each other and having a TFT formed at each intersection part thereof to drive a liquid crystal cell Clc, a data driver 83 to supply data to the data lines 55 of the liquid crystal display panel 57, a gate driver 84 to supply scan pulses to the gate lines 56 of the liquid crystal display panel 57, a timing controller 81 to which RGB data from an input line 90, synchronization signals H/V and main clock signals MCLK are input, a frame memory 88 connected between the timing controller 81 and the data driver 83, bit converters 89A and 89B, and a lookup table 82.

Please replace paragraph **[0092]** with the following amended paragraph:

[0092] FIG. 11 represents an exemplary apparatus for driving a liquid crystal display according to a fifth embodiment of the present invention. Referring to FIG. 11, an apparatus for driving the liquid crystal display may include a liquid crystal display panel 57 having data lines 55 and gate lines 46 crossing each other and having a TFT formed at each intersection part thereof to drive a

liquid crystal cell Clc, a data driver 113 to supply data to the data lines 55 of the liquid crystal display panel 57, a gate driver 114 to supply scan pulses to the gate lines 56 of the liquid crystal display panel 57, a timing controller 111 to control the data driver 113 and the gate driver 114, a bit converter 119 to convert n-bit data from an input line 120 into (n-m) bit data, and a frame memory118 and a lookup table [[102]] 112 connected between the bit converter 119 and the timing controller 111.

Please replace paragraph **[0112]** with the following amended paragraph:

[0112] Alternatively, referring to FIG 15, an apparatus for driving a liquid crystal display according to a seventh embodiment of the present invention may include a liquid crystal display panel [[157]] 57 having data lines [[155]] 55 and gate lines [[156]] 56 crossing each other and having a TFT formed at each intersection part thereof to drive a liquid crystal cell Clc, a data driver [[153]] 53 to supply data to the data lines [[155]] 55 of the liquid crystal display panel [[157]] 57, a gate driver [[154]] 54 to supply scan pulses to the gate lines [[156]] 56 of the liquid crystal display panel [[157]] 57, a timing controller [[151]] 51 for comparing the most significant 7-bits in the 8-bit source data to modulates the data and, in addition, generating timing control signals DDC and GDC, and first and second frame memories [[158]] 58 and [[159]] 59 connected between an input line [[160]] 60 and the timing controller [[151]] 51.

Please replace paragraph **[0113]** with the following amended paragraph:

[0113] The liquid crystal display panel [[157]] 57 may have liquid crystals injected between two glass substrates, and the data lines [[155]] 55 and the gate lines [[156]] 56 may be formed to

perpendicularly cross each other on a lower glass substrate. The TFT provided at the intersection part of the data lines [[155]] 55 and the gate lines [[156]] 56 may supply the data through the data lines [[155]] 55 to the liquid crystal cell Clc in response to the scan pulse from the gate lines [[156]] 56. To this end, the gate electrode of the TFT may be connected to the gate lines [[156]] 56 while the source electrode thereof may be connected to the data lines [[155]] 55. The drain electrode of the TFT may be connected to a pixel electrode of the liquid crystal cell Clc.

Please replace paragraph **[0114]** with the following amended paragraph:

[0114] The data driver [[153]] 53 may include a shift register to sample a dot clock of the timing control signal DDC, a register to temporarily store data; a latch to store the data by lines and to simultaneously output the stored data of one line in response to the clock signal from the shift register, a digital-to-analog converter to select a positive/negative gamma voltage in correspondence to the digital data value from the latch, a multiplexor to select a data line [[155]] 55 to which the data are outputted from the digital-to-analog converter, and an output buffer connected between the multiplexor and the data line. The data driver [[153]] 53 may be supplied with red (R), green (G), and blue (B) modulated data Mdata modulated by the timing controller [[151]] 51 and may supply the modulated data Mdata to the data lines [[155]] 55 of the liquid crystal display panel [[157]] 57 in response to a data control signal DDC from the timing controller [[151]] 51.

Please replace paragraph **[0115]** with the following amended paragraph:

[0115] The gate driver [[154]] 54 may include a shift register to sequentially generate scan

pulses in response to a gate control signal GDC received from the timing controller [[151]] 51, and a level shifter to shift a voltage of the scan pulse into a level suitable for driving the liquid crystal cell Clc.

Please replace paragraph **[0116]** with the following amended paragraph:

[0116] The timing controller [[151]] 51 may compare the most significant 7-bits of the source data of the current frame Fn with those of the previous frame Fn-1, and may select the modulated data Mdata in correspondence to the result of the comparison, wherein the source data may be input from the first and second frame memories [[158]] 58 and [[159]] 59. The modulated data Mdata selected by the timing controller [[151]] 51 may be input to the data driver [[153]] 53. Further, the timing controller [[151]] 51 may generate a gate control signal GDC to control the gate driver [[154]] 54 and a data control signal DDC to control the data driver [[153]] 53 by using horizontal and vertical synchronization signals H and V and a main clock MCLK.

Please replace paragraph **[0117]** with the following amended paragraph:

[0117] The first frame memory [[158]] 58 may store the data received from the input line [[160]] 60 for one frame interval, and may supply the stored RGB data of the current frame Fn to the second frame memory [[159]] 59 and the timing controller [[151]] 51. The second frame memory [[159]] 59 may store the data received from the first frame memory [[158]] 58 for one frame interval, and may supply the stored RGB data of the previous frame Fn-1 to the timing controller [[151]] 51.

Please replace paragraph **[0118]** with the following amended paragraph:

[0118] Alternatively, an interface circuit may be installed between the input line [[160]] 60 and the frame memory [[158]] 58 to reduce data bus lines, wherein the interface circuit may adopt an interface system, such as a Low Voltage Differential Signaling LVDS system, a Transition Minimized Differential Signaling TMDS system, or Reduced Swing Differential Signaling RSDS system etc. Further, a bit conversion circuit or a 7-bit bus line may be installed at the input terminal of the first frame memory [[158]] 58 or the output terminals of the first and second frame memories [[158]] 58 and [[159]] 59, wherein the bit conversion circuit casts away a least significant bit '2°' in the 8-bit source data and only takes most significant 7-bits.

Please replace paragraph **[0132]** with the following amended paragraph:

[0132] FIG. 19 is a circuit diagram representing an exemplary comparator shown in FIG. 18 according to the present invention. In FIG. 19, the comparator 259 may include first to seventh XOR gates 270A to 270G, a logic circuit receiving an output signal from each of the first to seventh XOR gates 270A to 270G to output a one-bit logical value, and a data outputter to supply the source RGB data of the current frame Fn to the data driver [[153]] 253 or to supply the source RGB data of the current frame Fn and the source RGB data of the previous frame Fn-1 to the timing controller 251 in response to the logical signal from the logic circuit 272.